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APPLICATION NO.	FI	LING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/694,913	1	10/29/2003	Gen Sasaki	244176US2 DIV	4521	
22850	7590	12/12/2006		EXAM	EXAMINER	
C. IRVIN M	CCLEL	LAND	TRAN, NHAN T			
OBLON, SPI	VAK. MO	CCLELLAND, MAI	ER & NEUSTADT, P.C.			
1940 DUKE			ART UNIT	PAPER NUMBER		
ALEXANDR	IA, VA	22314		2622		

DATE MAILED: 12/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)
	•	10/694,913	SASAKI, GEN
Office Action Summary		Examiner	Art Unit
		Nhan T. Tran	2622
	The MAILING DATE of this communication ap	ppears on the cover sheet with the	correspondence address
Period fo	• •	. V IO 057 TO 5VDID5 - MONTH	(O) OD TUDTY (OO) DAYO
WHIC - Exter after - If NC - Failu Any	ORTENED STATUTORY PERIOD FOR REPI CHEVER IS LONGER, FROM THE MAILING I nsions of time may be available under the provisions of 37 CFR 1. SIX (6) MONTHS from the mailing date of this communication. Operiod for reply is specified above, the maximum statutory period are to reply within the set or extended period for reply will, by staturely received by the Office later than three months after the mailined patent term adjustment. See 37 CFR 1.704(b).	DATE OF THIS COMMUNICATIO .136(a). In no event, however, may a reply be tid d will apply and will expire SIX (6) MONTHS from te, cause the application to become ABANDON	N. mely filed n the mailing date of this communication. ED (35 U.S.C. § 133).
Status			
1)🖂	Responsive to communication(s) filed on 28 s	September 2006.	
2a)⊠	This action is FINAL . 2b) This	is action is non-final.	
3)	Since this application is in condition for allowa	ance except for formal matters, pr	osecution as to the merits is
	closed in accordance with the practice under	Ex parte Quayle, 1935 C.D. 11, 4	53 O.G. 213.
Dispositi	ion of Claims		
4)	Claim(s) 15,16 and 28 is/are pending in the a	application.	
,	4a) Of the above claim(s) is/are withdra		
5)🖂	Claim(s) 28 is/are allowed.		
6)⊠	Claim(s) <u>15</u> is/are rejected.		
•	Claim(s) <u>16</u> is/are objected to.		
8)	Claim(s) are subject to restriction and/	or election requirement.	
Applicati	ion Papers		
9)	The specification is objected to by the Examin	ner.	
,	The drawing(s) filed on is/are: a) ac		Examiner.
	Applicant may not request that any objection to the	e drawing(s) be held in abeyance. Se	ee 37 CFR 1.85(a).
	Replacement drawing sheet(s) including the corre	ction is required if the drawing(s) is ol	bjected to. See 37 CFR 1.121(d).
11)	The oath or declaration is objected to by the E	Examiner. Note the attached Office	e Action or form PTO-152.
Priority (under 35 U.S.C. § 119		
	Acknowledgment is made of a claim for foreig	n priority under 35 U.S.C. § 119(a	a)-(d) or (f).
	☐ All b)☐ Some * c)☐ None of:		
	1. Certified copies of the priority documer	nts have been received.	
	2. Certified copies of the priority documer	nts have been received in Applica	tion No
	3. Copies of the certified copies of the price.		ed in this National Stage
	application from the International Burea		
* \$	See the attached detailed Office action for a lis	st of the certified copies not receiv	ea.
Attachmen	ıt(s)		
	te of References Cited (PTO-892)	4) Interview Summar	
	te of Draftsperson's Patent Drawing Review (PTO-948) mation Disclosure Statement(s) (PTO/SB/08)	Paper No(s)/Mail D 5) Notice of Informal	
	er No(s)/Mail Date	6) Other:	

Application/Control Number: 10/694,913 Page 2

Art Unit: 2622

DETAILED ACTION

Response to Arguments

- 1. Applicant's arguments, filed 9/28/2006, with respect to new claim 28 have been fully considered and are persuasive.
- 2. Applicant's arguments, filed 9/28/2006, with respect to claim 15 have been considered but are most in view of the new ground of rejection.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 10/19/2006 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 4. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kapan (US 5,291,293) in view of Heller et al. (US 6,396,539 B1).

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Application/Control Number: 10/694,913

Art Unit: 2622

Page 3

Regarding claim 15, Kapan discloses an image processing circuit of an image input device (Fig. 1) which performs a predetermined image processing (amplifying) of an image photographed by an image pickup device having a pixel array (pixel array 10, 12) in said image input device, said circuit comprising:

a real time processing unit (combined circuits 20-26) in which a predetermined general image processing of a pixel data in the image photographed by said image pickup device and inputted sequentially is performed by real time processing (see Fig. 1; col. 2, lines 21-44);

a main memory (36) disposed outside of said real time processing unit that stores a pixel data outputted from at least said real time processing unit (20-26), in image frame units (col. 2, line 65 - col. 3, line 7 and col. 4, lines 19-27; note that each line of pixels produces a frame since "frame" is broadly recited in the claim), and stores defective pixel addresses (col. 3, lines 4-7), wherein, said real time processing unit further comprises a defective pixel compensation block (26) that reads the defective pixel addresses (via switch enable line from control processor 34) stored in said main memory (36), and performs defective pixel compensation (by switching to either amplifier 22 or 20) when a pixel address of a pixel data residing in the image matches said defective pixel address, said defective pixel compensation performed in the pixel array sequence order (see Fig. 1 and col. 2, line 59 – col. 3, line 62, and note that the compensation is performed in sequence order by reading out the pixels in sequence and then compensating defective pixels in real time).

Application/Control Number: 10/694,913

Art Unit: 2622

Although Kapan discloses that the defective pixel locations (addresses) are stored in the main memory (36), Kapan does not explicitly disclose that the defective pixel addresses are stored in a pixel array sequence order (i.e., a tabular table) having an order of the pixel array in said image input device. In the same field of endeavor for compensating defective pixels of an image sensor, Heller teaches a practice for storing defective pixel addresses in a tabular table which corresponds to pixel array sequence order of an image sensor (see Heller, Fig. 2, col. 8, lines 40-45).

Page 4

Therefore, it would have been obvious to one of ordinary skill in the art to arrange and store the defective pixel addresses in Kapan in form of a pixel array sequence order such as a tabular table in view of the teaching of Heller so that the image processing circuit would quickly retrieve and map the defective addresses for defective compensation in real time.

Allowable Subject Matter

- 5. Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
- 6. Claim 28 is allowed.

The following is an examiner's statement of reasons for allowance:

For both claims 16 & 28, the prior art of record fails to teach or fairly suggest the combination of all limitations of each of claims 16 & 28 that includes "...said defective pixel compensation block of said real processing unit comprises a shift register

Application/Control Number: 10/694,913 Page 5

Art Unit: 2622

with a plurality of registers connected in series, to which defective pixel addresses stored in said main memory are inputted sequentially, and a comparator connected to a rearmost stage of said shift register in which an address count value of a pixel data inputted sequentially is compared with a defective pixel address provided from said rearmost stage and, when a match is found, a defective pixel timing signal is outputted, said shift register holds a defective pixel address, and output of said rearmost stage is looped to an input terminal of a foremost stage, said comparator is a comparator in which an address count value of a pixel data inputted sequentially is compared with a defective pixel address provided from said rearmost stage and, when a match is found, a shift timing signal and a defective pixel timing signal are outputted, and shift of said shift register is executed by said shift timing signal provided from said comparator."

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

Application/Control Number: 10/694,913 Page 6

Art Unit: 2622

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Application/Control Number: 10/694,913

Art Unit: 2622

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Page 7

NHAN T. TRAN Patent Examiner

SUDER PATENT EXAMINER